IN THE CLAIMS

Each claim of the application is set forth below with a parenthetical notation immediately following the claim number indicating the claim status. The Examiner's entry of the claim amendments under Section 1.121 is respectfully requested.

1 – 19. (CANCELLED)

20. (CURRENTLY AMENDED) A method for fabricating a semiconductor device with a plurality of field-effect transistors comprising:

forming a first device region, selected from the group consisting of a source region and a drain region, of a first field-effect transistor on a semiconductor layer;

forming a second device region, selected from the group consisting of a source region and a drain region, of a second field-effect transistor on said semiconductor layer;

forming a first channel region over and in contact with said first device region, wherein said first channel region has an opposite conductivity type than the first device region;

forming a second channel region over and in contact with said second device region, wherein said second channel region has an opposite conductivity type than the second device region;

forming a gate adjacent said first channel region for said first field-effect transistor, wherein said gate has a first predetermined gate oxide thickness; and

forming a gate adjacent said second channel region for said second field-effect transistor, wherein said gate has a second predetermined gate oxide thickness, and wherein said first predetermined thickness is different than the second predetermined thickness.

21. (ORIGINAL) The method of claim 20 including the additional step of configuring the first and the second device regions, and the first and the second gate regions into a circuit comprising two MOSFETs.

22. (ORIGINAL) The method of claim 20 wherein the step of forming the gate having the first predetermined gate oxide thickness and the step of forming the gate having the second predetermined gate oxide thickness, comprises:

forming a gate for the first field-effect transistor, wherein said gate has a first predetermined gate oxide thickness;

forming a gate for the second field-effect transistor, wherein said gate has a first predetermined gate oxide thickness;

removing the oxide from said gate of the first field-effect transistor;

forming gate oxide material on said gate for said first field-effect transistor;

forming gate oxide material on said gate for said second field-effect transistor; and

such that the gate oxide of the first field-effect transistor has a thickness less than the thickness of the gate oxide for the second field-effect transistor.

23. (ORIGINAL) The method of claim 20 wherein the first and the second field-effects transistors can withstand different gate input voltages as a consequence of the differing predetermined gate oxide thickness.

24. (CURRENTLY AMENDED) A method for fabricating a semiconductor device with a plurality of transistors comprising:

forming first and second spaced-apart diffusion regions on a semiconductor layer;

forming a first channel ~~third semiconductor~~ region over and in contact with said first diffusion region, wherein said first channel ~~third semiconductor~~ region has an opposite conductivity type than said first diffusion region;

forming a second channel ~~fourth semiconductor~~ region over and in contact with said second diffusion region wherein said second channel ~~fourth semiconductor~~ region has an opposite conductivity type than said second diffusion region;

forming a first gate oxide of a first predetermined thickness adjacent said first channel ~~third semiconductor~~ region;

forming a second gate oxide of a second predetermined thickness adjacent said second channel ~~fourth semiconductor~~ region, wherein the first predetermined thickness is different from the second predetermined thickness;

forming fifth and sixth semiconductor regions, each positioned over one of said first ~~third~~ and said second ~~fourth semiconductor~~ channel regions, such that said first channel region ~~third~~ and said fifth region ~~regions~~ are vertically aligned with one of said first and said second regions, and such that said second channel region ~~fourth~~ and said sixth region ~~regions~~ are vertically aligned with the other of said first and second regions, the resulting

structure providing two transistors with a substantially vertical current flow through the first and the second channel regions.

25. (CURRENTLY AMENDED) The method of claim 24 wherein the step of forming the first gate oxide of a first predetermined thickness adjacent the first channel ~~third semiconductor~~ region and the step of forming the second gate oxide of the second predetermined thickness adjacent the second channel ~~fourth semiconductor~~ region comprises:

forming a first gate oxide of a first predetermined thickness adjacent said first channel ~~third semiconductor~~ region;

forming a second gate oxide of said first predetermined thickness adjacent said second channel ~~fourth semiconductor~~ region;

removing said first gate oxide;

forming a third gate oxide of a second predetermined thickness adjacent said first channel ~~third semiconductor~~ region;

forming said third gate oxide of said third predetermined thickness adjacent said second channel ~~fourth semiconductor~~ region; and

wherein the gate oxide thickness adjacent said second channel ~~fourth semiconductor~~ region is the sum of said first predetermined thickness plus said second predetermined thickness.

26. (CURRENTLY AMENDED) The method of claim 24 wherein the first and the second gate oxides are associated with a first and a second MOSFET, and wherein said first and said second MOSFETs form a complementary ~~complimentary~~ MOSFET device, ~~and wherein said third and said fourth gates are associated with a third and a fourth MOSFET, respectively, and wherein said third and said fourth MOSFETs form a second complimentary MOSFET device;~~ and wherein the gate terminals of said first ~~complimentary~~ MOSFET ~~device have~~ has a first breakdown voltage related to the first predetermined thickness, and wherein the gate terminals of said second MOSFET ~~device have~~ has a second breakdown voltage related to the second predetermined thickness.